Name of Subject :	Digital Electronics	Semester : 3 rd
Name of faculty :	Anita Rani	Branch : Computer

week	Lecture	Name of Topic	Experiment
1st	1 st	Introduction to Digital Electronics, Distinction between analog and digital signal.	Introduction with digital Lab equipments
	2^{nd}	Applications and advantages of digital signals	
	3rd	Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary and vice-versa.	
2nd	4th	Binary addition and subtraction including binary points. 1's and 2's complement method of addition/subtraction.	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive
	5th	Concept of code, weighted and non- weighted codes, examples of 8421, BCD, excess-3 and Gray code.	NOR(EXNOR) gates
	бth	Concept of parity, single and double parity and error detection.	
3rd	7th	Concept of negative and positive logic	Realization of logic functions with
	8th	Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR, EXOR Gates,	the help of NAND or NOR gates
	9th	NAND and NOR as universal gates.	
4 th	10th	Introduction to TTL and CMOS logic families	Revision and viva-voce
	11th	Revision	
	12 th	Postulates of Boolean algebra, De Morgan's Theorems.	
5 th	13 th	Implementation of Boolean (logic) equation with gates	To design a half adder using XOR and NAND gates and verification of
	14 th	Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits.	its operation
	15th	K-Map Practice and revision	
6th	16 th	Sessional Test	Construction of a full adder circuit
	17th	Half adder, design and implementation.	using XOR and NAND gates and verify its operation
	18 th	Full adder circuit , design and implementation and 4 bit adder circuit	

7 th	19th	Basic functions and block diagram of MUX	Verification of truth table for
0.1	4	and DEMUX with different ICs.	encoder and decoder ICs, Mux and
	20^{th}	Four bit decoder circuits for 7 segment	De-Mux
	e i st	display and decoder/driver ICs.	-
	21 st	Basic functions and block diagram of	
	22 nd	Encoder	Derivier and size and a
8th	22 23 rd	RevisionConcept and types of latch with their	Revision and viva-voce
	23	working and applications	
	24 th	Difference between a latch and a flip flop	
	24	Difference between a fater and a mp hop	
9th	25 th	Operation using waveforms and truth tables	Verification of truth table for
		of RS, T, D,	positive edge triggered, negative
	26 th	Master/Slave JK flip flops.	edge triggered, level triggered IC
	27^{th}	Introduction to Asynchronous and	flip-flops (At least one IC each of D
	4	Synchronous counters .	latch, D flip-flop, JK flip-flops).
10th	28 th	Binary counters and divide by N ripple	Use of Asynchronous Counter ICs
	aoth	counter	(7490 or 7493)
	29 th	Decade counter and ring counter	
11 th	30 th 31 st	Revision	-
11	$\frac{31}{32^{nd}}$	Revision	-
	32 33 rd	Sessional Test Introduction and basic concepts including	-
	55	introduction and basic concepts including	
		shift left and shift right. Serial in parallel	
		out, serial in serial out,	
12th	34th	parallel in serial out, parallel in parallel out.	To design a 4 bit ring counter and
	35 th		verify its operation.
	35 36 th	Universal shift register Revision	
13 th	30 37 th	Working principle of A/D and D/A	To design a 4 bit SISO, SIPO, PISO,
15	57		PIPO shift registers using JK/D flip
		converters and Applications of A/D and	flops and verification of their
	aoth	D/A converter.	operation
	38 th	Binary Weighted D/A converter and R/2R	1
	th	ladder D/A converter	4
	39 th	Stair step Ramp A/D converter, Dual Slope	
	4	A/D converter	
14 th	40 th	Successive Approximation A/D Converter	Revision and Viva
	41 st	Memory organization,.	
	42^{nd}	classification of semiconductor memories	
		(RAM, ROM, PROM, EPROM,	
	1. a. #d	EEPROM), static and dynamic RAM,	
15th	43 rd	Introduction to 74181 ALU IC	Revision and viva
	44 th	Revision	4
16th	45 th	Sessional Test	
	46th	Revision	Revision and viva
	47 th	Revision	4
	48th	Revision	